

Figure 1

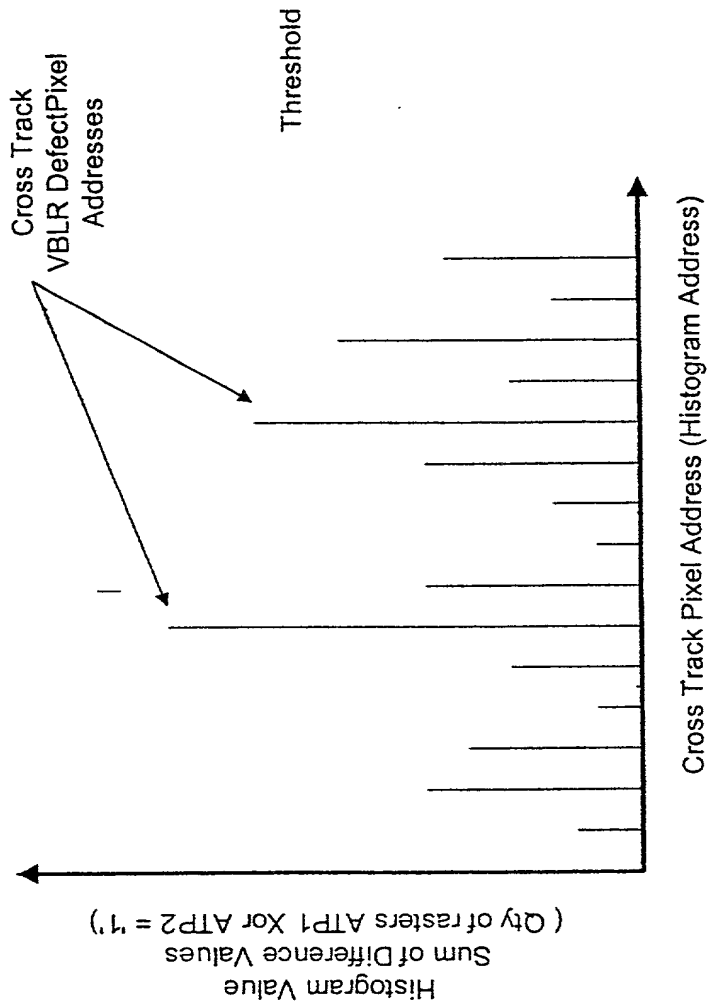


Figure 2

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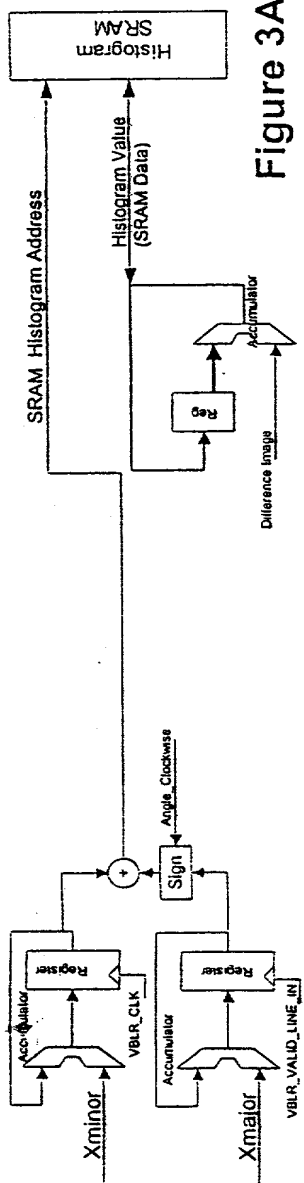


Figure 3A

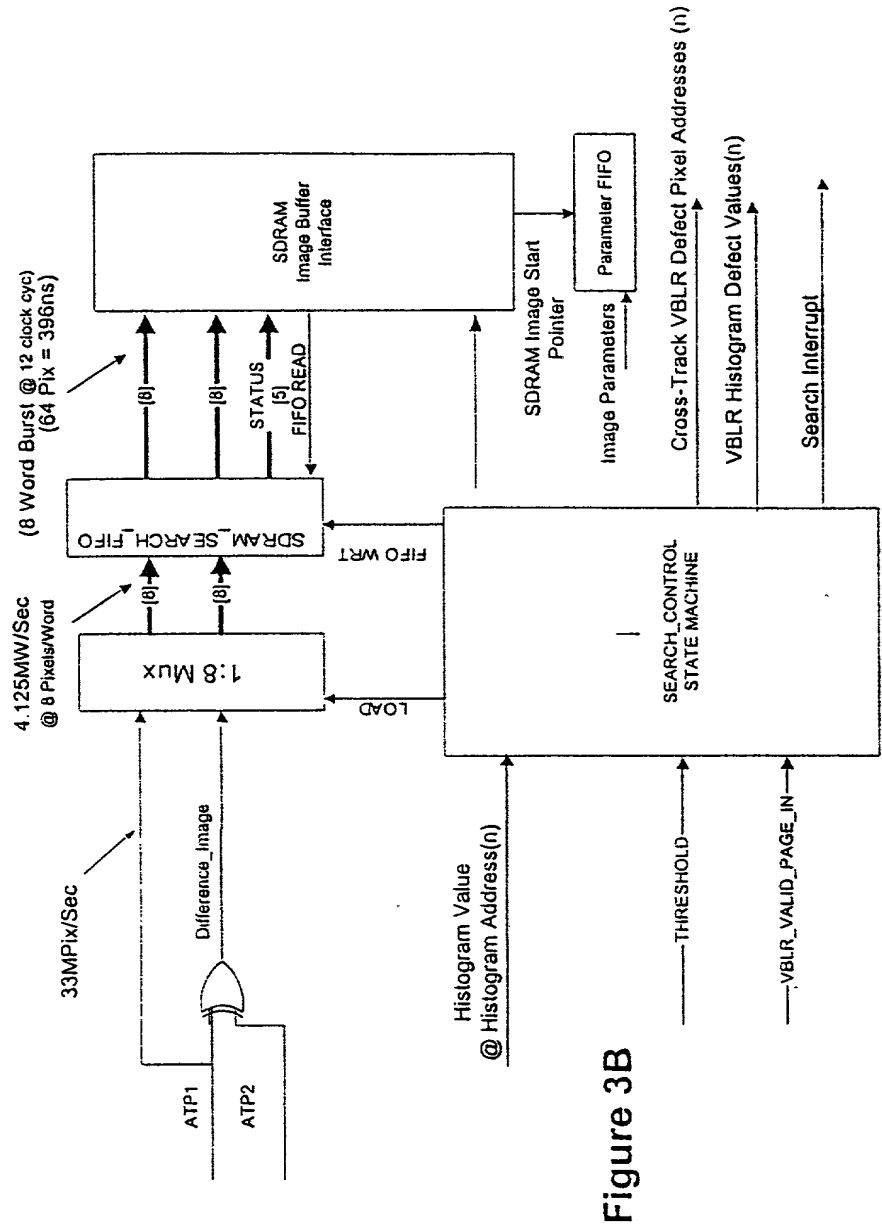


Figure 3B

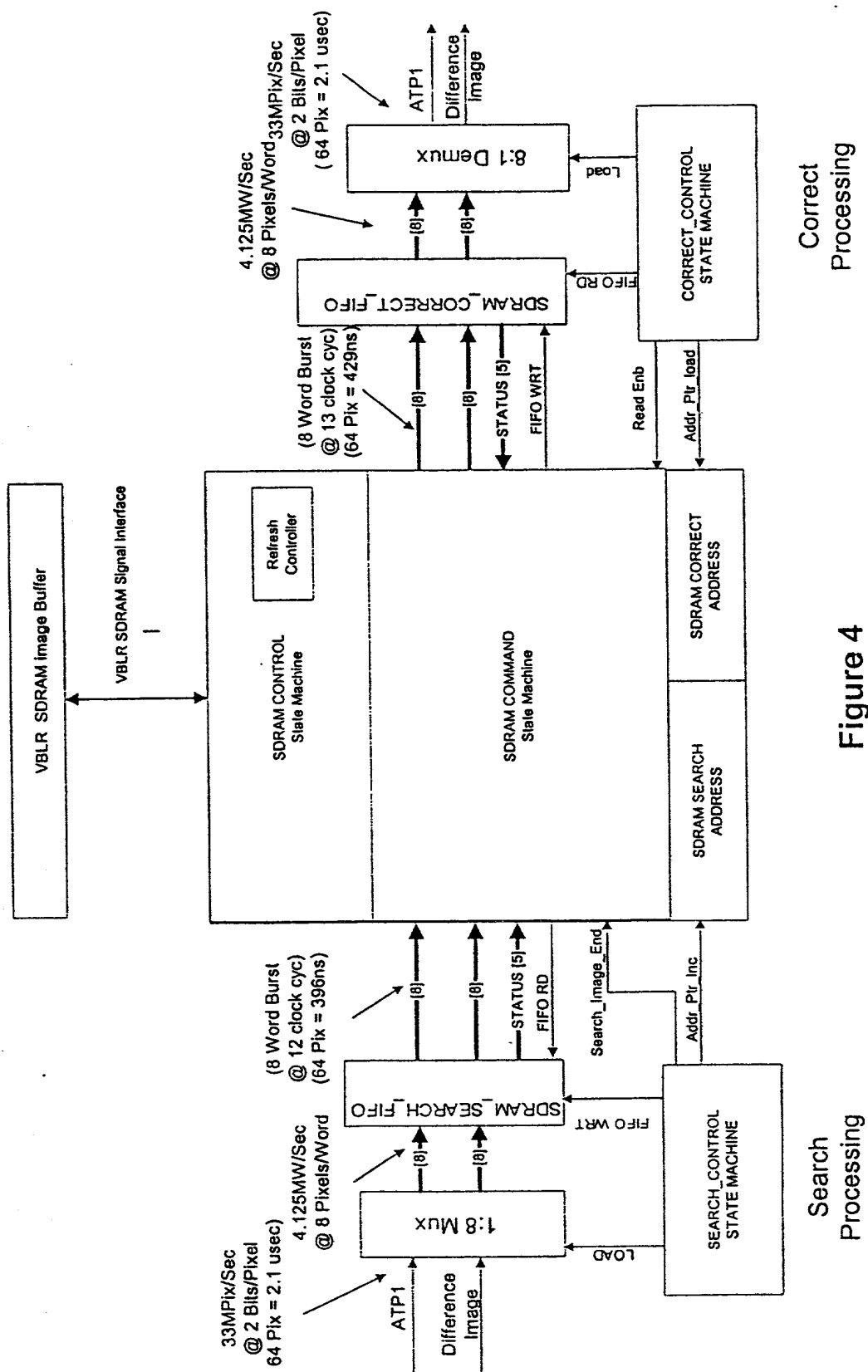
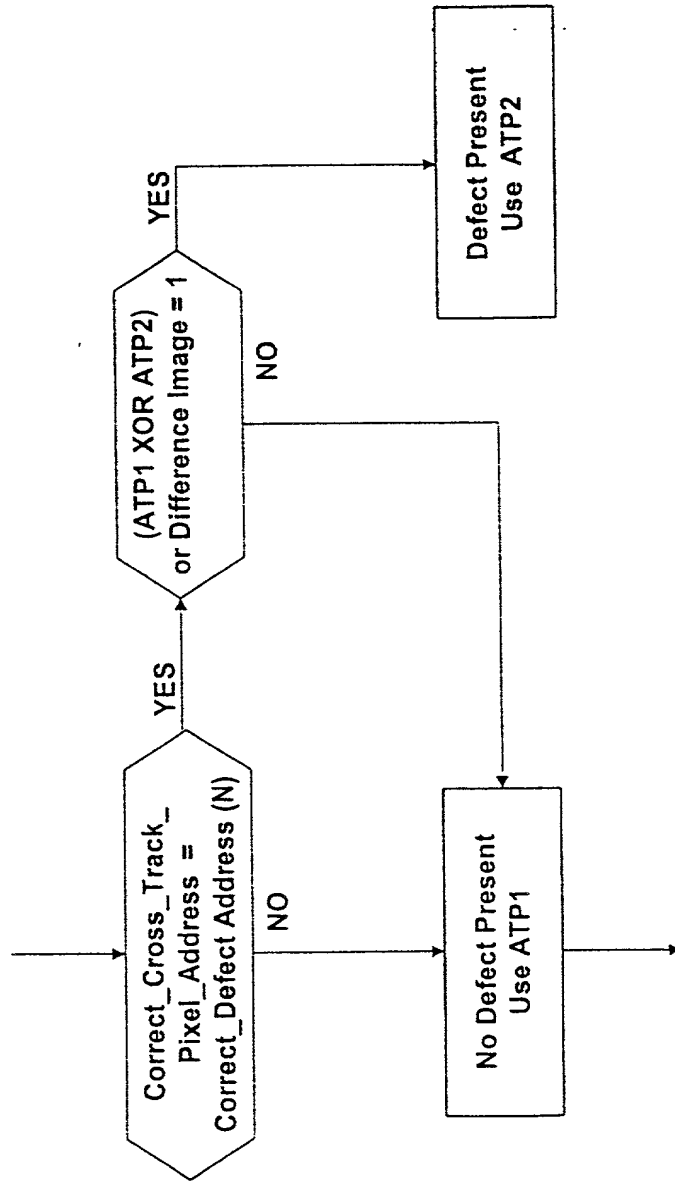


Figure 5



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TO VBLR SDRAM
INTERFACE

Figure 6

